# DESIGN A MICRO-OHMMETER FOR MEASURING VERY SMALL RESISTANCE

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# Abstract

In our paper the micro-ohmmeter in This circuit will be used for measuring very small resistances without applying large currents. The mili-voltage value will be used in this paper as well. Anyway, the Achievement of the circuit consists of two parts, simulation by software, and hardware. This paper is going to describe all steps one by one with calculation, simulation and hardware results.

### Introduction

In this circuit, we are going to design a micro-ohmmeter that could be measure low amplified by an amplifier then rectified using rectification circuit. This circuit can be used to track shorting in printed circuit boards without affecting the sensitive components on it. The circuit consists of six main parts which are: (source, Kelvin probes, Differential Amplifier, Phase sensitive detector (PSD),Voltage-Controlled Oscillator (VCO), Muting Detector (Comparator)).We are going to explain all parts and the function of them in this report.

The aim of this experiment :-

- Design and test a lock-in Amplifier based micro-ohmmeter.
- Extraction of resistance measurement via the 4WKP, in order to filter inaccuracies.
- Understand the concept of IA in order to assure reasonable rejection and high common-mode range.



- Achievement of 1.1 KHz oscillation from the Source (i.e., oscillator, Quadrature & Attenuator) in terms of peak-to-peak form of less than 200mV.
- Achieve and output of a waveform around 10 KHz, in terms of audible signals from the microphone.

#### System Block Diagram



Figure (1) Block diagram of the instrument design

#### Source

The source consists of (Oscillator), (Quadrature Divider) and (Balanced Attenuator) as Shown in figure (2). [5]



(Figure 2 Oscillator, Quadrature Divider and Attenuator circuit)

#### - Oscillator

An oscillator is an electronic circuit that produces a repetitive electronic signal, often a sine wave. Oscillators designed to produce a high-power AC output from

a DC supply are usually called inverter. There are many types of electronic oscillator; One of them the 555 Timer IC can be connected in its Monostable mode thereby producing a precision timer of a fixed time duration, or in its Bistable method to yield a Flip-flop type switching action [2]. The connections for astable or free-running operation. Together the trigger& threshold inputs are linked directly to the capacitor. Also there is an Extra resistor,  $R_1$ , connected between the capacitor and the discharge transistor to slow the discharge.



(Figure 3 The basic 555 timer diagram)

The beginning of the source which generates 1.1KHz frequency, at this frequency  $R_2$  equals 130K, the end result of output of oscillator as shown in figure (4,5). Controlling the charging time (controlling the frequency) via  $R_1$  and  $R_2$ . Regulatory the discharging time via  $R_1$ . After this comes the stage of Quadrature Divider.

The total period is the sum of the charge and discharge time t

$$T = 0.693(R_2 + 2R_1) C.$$

$$AT \Longrightarrow U1 \Longrightarrow F = \frac{1}{T} = \frac{1}{250m} = 0.004 * 10^6 = 4 \text{ KHZ}$$
  
Thigh=0.693\*C<sub>3</sub>\*(R<sub>1</sub>\*R<sub>2</sub>)  
Theorem = 0.693\*C<sub>3</sub>\*R<sub>1</sub>



 $Period = T_{high} + T_{low} = 0.693 * C_3 * (R_2 + 2R_2)$ 

$$F = \frac{1}{T} = \frac{1.443}{C_3 \times (R_2 + 2R_1)}$$
  
1.1 khz =  $\frac{1.443}{10 \times 10^{-9} \times (2 * 1k\Omega + R_2)} \implies R_2 = 129.2 \text{ k}\Omega \approx 130 \text{ k}\Omega$ 



**Oscillator**)

#### (Figure 5 The output of the

#### - Quadrature Divider

The Quadrature Divider as its name denotes to dividing by four, here it does divide the frequency of 4KHz by four resulting in a frequency of about 1KHz. The Balanced PI type Attenuator technically reduces the amplitude of the voltage by a fraction which is really determined with the R<sub>5</sub> value (Note: Voltage divider theorem and that resistance is in direct proportion with Voltage) prior to the signal getting to J<sub>4</sub>.

$$AT \Longrightarrow U2: A, B \Longrightarrow F = \frac{1}{T} = \frac{1}{1000 * 10^{-6}} = 1 * 10^3 = 1 KHZ$$









(Figure 7 Quadrature divider output(at 0 0 and 180 0)) (Figure 8 Quadrature divider output(at 90 0 and 270))

U1		U2,A		U2,B	
voltage	frequency	voltage	Frequency	Voltage	frequency
6.16 AC	1.025 HZ	4.88 AC	257.1HZ	6.40 AC	257.1HZ

#### - Balanced Attenuator

An attenuator is an electronic expedient that reduces the amplitude or power of a signal without noticeably distorting its waveform. An attenuator is effectively the opposite of an amplifier, though the two work by different methods. While an amplifier offers gain, an attenuator provides loss, or gain less than 1.Attenuators are usually passive devices made from simple voltage divider networks. Switching between different resistances forms adjustable stepped attenuators and continuously regulating ones using potentiometers.



The output signal should have peak-to-peak amplitude of not as much of 400mV. Together these values have a +/- 5% tolerance. The waveform frequency about 1.1 kHz. Then in this step the voltage will be reduced from 6V to 400mv peak to peak at which the value of  $R_5$  (75) was obtained by using Thevenin's theorem as shown below, The higher value of RL the higher the voltage across it

 $V_{out} = V_{in} *R_5/(R_3 + R_4 + R^5)$   $200mv = 6 R_5/(1.1K + 1.1K + R_5) \qquad R_5 = 75.86 \Omega$ Recalculate when the v<sub>in</sub> 4.88  $V_{out} = Vin * R_5/(R_3 + R_4 + R^5)$  $200mv = 4.88 * R_5/(1.1K + 1.1K + R_5) \qquad R_5 = 94 \Omega$ 

Calculate the (rather small) voltage we measured when a  $1m\Omega$  resistor is connected across  $R_5$ 

$$V_{out} = V_{in} * ((R_5 * R_L / R_5 + R_L) / R_3 + R_4 + (R_5 * R_L / R_5 + R_L))$$
  
$$V_{out} = 4.88 * \frac{0.00099}{1.1k + 1.1k + 0.00099} \qquad V_{out} = 2.22 \mu v$$

Aftar that we are going to calculate the voltage corresponding to 0.22, which the maximum resistance this device is intended.

$$V_{out} = V_{in} * R_L / (R_3 + R_4 + R_L)$$
  $V_{out} = 0.000485v$ 

We used  $0.22\Omega$  resistor as a load resistor so we've got 0.485mv voltage source at point J<sub>4</sub> as required.

# **Differential Amplifier**

An instrumentation amplifier is a gentle of differential amplifier that has been outfitted with input buffers, which eliminate the requirement for input impedance matching and thus make the amplifier particularly suitable for use in measurement and test equipment. Additional characteristics include very low DC offset, low drift, low noise, very high open-loop gain, very high common-mode



rejection ratio, and very high input impedances [4]. Instrumentation amplifiers are used where excessive correctness and stability of the circuit both short- and long-term are essential. As the voltage value across the amplifier must be 200mV, will be easy to find by calculation that this value is 10 times greater . we can see the result of the calculate

$$R_{9} = \frac{Vout}{(V2+V1)} = \left(1 + \frac{2R1}{Rgain}\right) * \frac{R3}{R2}$$
$$\frac{2.4}{0.000446*2} = 1 + \left(\frac{2*10000}{Rgain}\right) * \frac{100}{10}$$
So R<sub>9</sub>=81KΩ

After the calculate  $R_9$ , so we used  $R_9=81k\Omega$ , in this time we found the gain is inversely proportion to  $R_9$ 

The question that we should think about is, Why we have distributed the gain, rather than using U3 to supply all the gain? Are there any disadvantages to doing this?

Because the value of the first stage is smaller than the next, otherwise we multiply the gain in ten times to get the good output. In the Figure below we can see the Real amplifier Circuit Test Result at  $J_5\&J_6$  with  $J_3$ . Moreover, we can see the gain of the differential stage it well be 10 rather than the normal 1, this is because

$$\frac{R_{19}}{R_{17}} = \frac{100K}{10K} = 10,$$
 also as the end result the ratio of the

resistances is 10 as well as the gain is 10 time.

 $R_{12}$  is different from the stated value by 1%. There is no effect at the output signal.



Any of  $R_{15, 16, 17, 19}$  are different from the stated value by 1%. The gain could increase & amplify by increasing or decreasing the value of any one of these resisters



(Figure 9 Real amplifier Circuit Test Result at J5&J6 with J3)

### Phase sensitive detector (PSD)

This device is responsible for the rectification process where the amplified AC signal get rectified to a DC signal. Further the rectification process a DC signal is obtained but with unwanted ripples as it shown in figure 8 which was denoted via pin J8 & 11. Bear in mind this is the second stage of amplification therefore it will be amplified by a gain of ten has been worked out. The components of the PSD are phase reversing switches which technical works using zero crossing reference, which makes the signal in the required manner. As the final outcome is required to be fully rectified which is can bee seen in figure (9), for this reason even numbers of switches are responsible for this task.

 $V_{PSD} = V_{SIG}V_L \sin(\omega_r t + \theta_{sig}) \sin(\omega_L t + \theta_{ref})$ 

In practice and simple words the PSD also ensures that the wanted signal is processed with elimination of unwanted signals, and the PSD becomes unique when it carries out the filtration of a signal of predetermined reference such as frequency and this cannot be obtain with alternatives technique of PSD such as



Diodes. Emphasizing the location of the PSD to be between the two op-amps and the third is to remove the spikes with the DC signal which are a result of  $C_7$ . In this circuit the phase reversing switch is located in the middle of the two op-amps and their third companion which results in the PSD, this is so in order to neglect switching spikes which are caused of released charges ( $C_7$  duty).



(Figure 10 circuit of Phase sensitive detector)

# The Synchronous Switch

This is the core of the whole design. The aim is fairly easy, but designing a phasereversing switch which does not inject not needed voltage spikes into the signal is surprisingly difficult. The main problem is that, to switch quickly and completely, the switching signal voltage is often quite large and has sharp transitions (SIMON BATESON).

A synchronous switch for rectified alternating circuits, the function of which be automatically synchronized on the crossing to zero of the load voltages at its terminals. This synchronous switch contains essentially a semi-conductor element selected from thyristors of a particular kind and possibly a diode. The semiconductor component comprises two essentials electrodes and a control electrode. This part can only be triggered at times when the polarity of the control voltage at the gate is the reverse of that of the first main electrode, and once triggered it after that remains blocked until the load current crossing it is reduced to zero. To provide an alternating current switch, the main electrodes might be linked to a rectifier bridge, and it may also be connected across a diode, and the devices thus formed can be used to interrupt each phase of a poly phase load current. In the Figure (11) it can be clearly seen the Synchronous Switch circuits.

#### Figure 11 The Synchronous Switch circuits

### **Output Reference – Ground 3V**

The major purpose of having this circuit is to create a platform for referencing the DC voltage signals by the LPF, rectifier, and the VCO. Technically here  $C_{12}$  capacitance is kept inaccessible by  $R_{32}$ , which in a sense makes the virtual ground reference. Looking up this section of the circuit concludes that it is potential divider theorem to be used to work out  $R_{31}$ , and as can be seen  $R_{32}$  &  $R_{33}$  are identical hence virtual ground voltage is  $V_3$ .







Figure (12) wiring diagram of Reference Ground

### Sallen-Key Equal Value low pass Filter

The signal which is the input to the LPF carries some noise and it's been passed through this filter in order to achieve a clean DC signal which is noiseless at J8, It couldn't be clearly smooth but contains glitches due to phase lags introduced in the differential amplifier stage. It will be contains noise, in the form of mains pickup, thermal noise and DC offset. To average all of these disturbances, we need a low pass filter to eliminate the ripples. The purposes of the low pass filter in this circuit to eliminate the ripples and just pass low frequency because the output DC of the amplifier was had ripples and this Undesirable so the output of the low pass filter will be pure and steady DC. When we measured between J9 and J<sub>11</sub> &R load=0.220hm we obtained pure and steady DC  $\approx$ 1.3V as shown in figure(14) and as input to Voltage-Controlled Oscillator (VCO) and we designed R20 and R<sub>22</sub> as following:

$$f = \frac{1}{2\pi RC}$$

 $R = \frac{1}{2\pi FC} = \frac{1}{2*5*0.1*10^{-6}} \qquad R = 322.3 \qquad R22 = R20 = 330$ 





(Figure 13 Real LPF Circuit Test Result at J9 with J11&R load=0.22ohm)

# Voltage-Controlled Oscillator (VCO)

In the this part of the design .A voltage-controlled oscillator (VCO) provides a periodic signal, more fore, is an electronic oscillator designed to be controlled in oscillation frequency according to the voltage input, the frequency could be changed by a variable (DC) control voltage at last the output from the comparator is further processed in the VCO, at this step the VCO implements the output from the comparator in an oscillating periodic signal form where the frequency of the produced signal is in comparison to the input feed into the VCO which denotes to range of the resistance to be measured in a range manner .[6] The system used in this part is the potential divider method where the DC output from the PSD and comparator in return switches the VCO to on status till the DC output from PSD circuit is under the reference voltage which is originally set up by the potential divider technique we can see the circuit of Controlled Oscillator (VCO) in figure (14) and The output of the integrator and comparator stages of the VCO as shown in figure (16) shows  $R_{38}$  and  $(j_{11})$  charge and discharge and (R) load=10 hm and figure(17) shows  $j_{12}$  with (j11) charge and discharge and r  $load = 0.22\Omega$ .



It is possible to obtained by the following equation:

$$F_0 = V_1 / 8RC (V_{th} - V_{th})$$
$$\mathcal{U}k = \frac{4.5 - 3}{8 \times 100 KC \times 1.5}$$
$$C = \frac{4.2 - 2.5}{8 \times 100 K \times \mathcal{U}k \times 1.5}$$

#### $= 225 \, pf$

, but in practical we used 220pf capacitor which is the closest available in the lap



Figure 14 Voltage-Controlled Oscillator (VCO) Circuit



figure(15)- R38& (j11) charge &dis charge &(R) load figure(16)j12 with (j11) charge &discharge &(R) load

# **Muting Detector (Comparator)**

The most important function in this step to mute the buzzer. When the measured resistor is bigger than  $0.22\Omega$ . How this process happens?, The principle of operation of this circuit depends on the process of Comparator When the measured resistor become high value, the output voltage of source will be increase the voltage at J9 becoming greater than the reference voltage 3v a result of that, the comparator U6:A will produce negative signal , this signal will enable the diode to pass signal. However, Thus at this voltage the transistor will be switched off because the transistor base voltage will always be less than the emitter voltage. So the charging and discharging of the capacitor will not continue which will mute the sound In the figure (17) below the circuit of the muting detector



Figure (17) muting detector circuit

$$V0 = \frac{Vi * R34}{R24 + R34}$$
$$4.5 = \frac{6 * R34}{10K + R34}$$

R<sub>34</sub>=30K

### Conclusion

The simulation of the design is achieved by check every signal in the circuit (inputs and outputs) and the suitable values of the components are selected which give the desired specification of the design without any cost.

The design is suitable to measure the resistor which has very low resistors maximum limit (0.22 ohm). The output frequency is muted by the comparator circuit when the values of the measured resistors more than 0.22 ohm which it is the aim of our design.

In An instrumentation amplifier circuit, there is one resistor controlling the value of gain

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